REMARKS

Claims 1-12 and 15 have been rejected under 35 U.S.C. 102(e) as being anticipated by Ohtani et al. (US 20030157758).

Claim 1 recites "forming one or more diffusion bit line regions in a semiconductor substrate; then thermally oxidizing the upper surface of the semiconductor substrate, thereby forming a bottom oxide layer over the upper surface of the semiconductor substrate and simultaneously forming bit line oxide regions over each of the one or more diffusion bit line regions; and then forming an intermediate dielectric layer over the bottom oxide layer and the bit line oxide regions." (Emphasis added.)

The Examiner argues that Fig. 65 of Ohtani et al. teaches the first two elements of Claim 1. Fig. 65 of Ohtani et al. refers to U.S. Patent No. 6,174,758 (Nachumovsky), which is assigned to the Applicant. The processes taught by Nachumovsky include the formation of an ONO structure, followed by the formation of diffusion bit lines, followed by the formation of bit line oxide. (Nachumovsky, Figs. 4-7.) The cited paragraphs [0003], [0005] and [0010] of Ohtani et al. do not dispute this process order. Thus, Ohtani et al. teach that the ONO structure (which includes a bottom oxide layer, an intermediate dielectric layer and a top oxide layer) is formed before the diffusion bit lines and the bit line oxide.

For this reason, Fig. 65 of Ohtani et al. teaches away from "forming ... diffusion bit line regions; then thermally oxidizing the upper surface of the semiconductor substrate, thereby forming a bottom oxide layer over the upper surface of the semiconductor substrate...; and then forming an

intermediate dielectric layer over the bottom oxide layer" as recited by Claim 1.

The Examiner also indicates that the third element of Claim 1 is taught by Figure 63 and paragraphs [0009] and 0020] of Ohtani et al. Because Ohtani et al. indicate that Figure 65 is prior art, and that Figure 63 is part of their invention, it is improper to combine the teachings of these Figures without proper motivation (because Figure 63 is attempting to overcome some deficiency of Figure 65).

Moreover, Figure 63 of Ohtani et al. is directed toward the deposition of a polysilicon film 33, which is used to form conductive gate electrodes. Thus, Figure 63 of Ohtani et al. does not seem to teach or suggest forming "an intermediate dielectric layer" as recited by Claim 1.

Moreover, the process sequence including Figure 63 of Ohtani et al. forms the bit line oxide films "by means of a CVD method or the like". (Ohtani et al., paragraph [0107]) Thus, Ohtani et al. explicitly teach away from "thermally oxidizing the upper surface of the semiconductor substrate, thereby forming ... bit line oxide regions over each of the one or more diffusion bit line regions" as recited by Claim 1.

In connection with Figs. 54-64 of Ohtani et al., it is also important to note that the bottom oxide layer 9a of ONO structure 9 is formed <u>before</u> bit line oxide film 19. Consequently, Ohtani et al. teach away from "forming a bottom oxide layer ... and <u>simultaneously forming</u> bit line oxide regions" as recited by Claim 1.

For these reasons, Claim 1 is not anticipated by Ohtani et al. Claims 2-12 and 15, which depend from Claim 1, are not anticipated by Ohtani et al. for at least the same reasons as Claim 1.

In addition, Claim 7 recites "implanting CMOS well regions through the intermediate dielectric layer and the bottom oxide layer". In contrast, Ohtani et al. teach that the CMOS well regions are formed before ONO structure 9 is formed. (Ohtani et al., Figs. 6 and 7.) For this additional reason, Claim 7 is not anticipated by Ohtani et al.

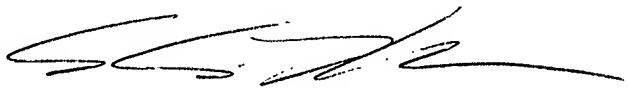
Claims 13-14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al.

Claims 13-14, which depend from Claim 1, are allowable over Ohtani et al. for at least the same reasons as Claim 1.

CONCLUSION

Claims 1-15 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested. If there are any questions, please telephone the undersigned at (925) 895-3545 to expedite prosecution of this case.

Respectfully submitted,



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